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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,405	03/26/2004	Christopher Young	15588US02	1337

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EXAMINER	
CHOW, CHARLES CHIANG	

ART UNIT	PAPER NUMBER
2618	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,405	YOUNG ET AL.	
	Examiner	**Art Unit**	
	Charles Chow	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-25, 27-38 and 40* is/are rejected.

7)☒ Claim(s) *13,26 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/3/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This is the first office action, acknowledging applicant's request for status of this application, dated 3/17/2006.

Information Disclosure Statement

2. The reference listed in the Information Disclosure Statement filed on dated 10/03/2003 have been considered by the examiner [see attached PTOL-1449 form].

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-8, 27-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Kang et al. (US 6,498,927B2).

For claim 1, Kang et al. [hereafter as Kang] teaches a method [steps in Fig. 9] for processing received signals in a communication system [the processing received signals by antenna 802 in wireless system 800 in Fig. 8 & abstract, the dynamic range in col. 9, lines 11-22], the method comprising

generating a plurality of upstream analog signals for a received signal [the down converted signal are output at each VGA of the plural variable gain amplifiers VGA 830, 846, 862 in Fig. 8; col. 8, lines 35-62; as the plural upstream analog signals];

acquiring upstream analog information related to at least a portion of said generated plurality of upstream analog signals [the power detectors 840, 856, 868 detecting, acquiring, the power level at the output of each VGA 830-862, step S910 in Fig. 9, col. 9,

lines 30-37; as the acquiring upstream analog information related to a portion of generated upstream analog signals]; and

adjusting a gain for said received signal using at least a portion of said acquired upstream analog information [reducing the gain of the selected stage, col. 9, lines 34-67 & the increasing the gain in col. 11, lines 24-37].

For claims 2, 28, Kang further teaches the comprising low pass filtering said received signal [the base band BB filter 852 is low pass filtering of received signal, to reduce SNR degradation in Fig. 8, col. 8, lines 56-62].

For claims 3, 29, Kang further teaches the wherein said generated plurality of upstream analog signals are narrowband analog signals [the BB filter 836, 852 filtered signal provides the narrow band signal, for the generated plural amplified signals].

For claims 4, 30, Kang teaches the further comprising acquiring at least one sample from at least a portion said generated plurality of upstream analog signals [the measuring power in step s910 & the power detecting power level at PD 820-868 of amplified signal at each VGA output, col. 9, lines 5-22; the received by gain controller 894 & AGC 884 via 876, as the processor].

For claims 5, 31, Kang teaches the further comprising computing a power based on said acquired at least one sample [the computing RSSI 892 based on the status gain_rpt 898 from gain controller 899 to gain calibration 899, as processor; the rssi is in dBm, power unit].

For claims 6, 32, Kang teaches the further comprising determining when at least one of said generated plurality of upstream analog signals is clipped [the above upper limit of signal level 1020, clipped, the gain controller, as processor, decreases the gain, col. 10, lines 48-58, Fig. 10B].

For claims 7, 33, Kang teaches the further comprising generating an intermediate gain based on said computed power of said acquired at least one sample [the intermediate gain change in steps s940 or s950, then process looping upwards to S910, before final gain, Fig. 9].

For claims 8, 34, Kang teaches the further comprising applying said generated intermediate gain to said at least one of said generated plurality of upstream analog signals [the reducing the gain stage by predetermined gain step size at s940, s950, Fig. 9, as the applying said intermediate gain].

For claim 27, Kang teaches a system for processing received signals in a communication system [the signal received by antenna 802 in wireless system 800 in Fig. 8 & abstract, the dynamic range in col. 9, lines 11-22], the system comprising

a receiver [803] that generates a plurality of upstream analog signals for a received signal [the down converted signal are output at each VGA of the plural variable gain amplifiers VGA 830, 846, 862 in Fig. 8; col. 8, lines 35-62];

at least one processor [gain controller 828, AGC 884] that acquires upstream analog information related to at least a portion of said generated plurality of upstream analog signals [the power detectors 840, 856, 868 detecting, acquiring, the power level at the output of each VGA 830-862, step S910 in Fig. 9, col. 9, lines 30-37; as the acquiring upstream analog information related to a portion of generated upstream analog signals]; and

at least one automatic gain controller [828, col. 9, line 37] that adjusts a gain for said received signal using at least a portion of said acquired upstream analog information [the reducing the gain of the selected stage, col. 9, lines 34-67 & increasing the gain col. 11, lines 24-37].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9-11, 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Brobston et al. (US 7,031,409 B2).

For claims 9, 35, Kang teaches the computing the accurate rssi 892, but fails to teach the comparing with defined power values.

Brobston et al. [Brobston] teaches the comparing said computed power to a plurality of defined power values [the computed power sample from output of 333 is compared with the program threshold value in register 335 at 341, the program threshold values are the defined power values; to determined the saturation at 342, for controlling the digitally multiplied gain, Fig. 3, col. 10, lines 29-42 & col. 8, lines 30-37, the agc for dynamic range in abstract, title], the agc 215 is processor controlled FPGA device [col. 7, lines 40-45] & with software programmability [col. 12, lines 30-32]. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang with Brobston's comparing the calculated power samples to the threshold value, in order to determine & reduce signal saturation.

For claims 10, 36, Kang teaches the computing the accurate rssi 892, but fails to teach the selecting a gain based on a comparable power value of said plurality of defined power values.

Brobston teaches the selecting a gain based on a comparable power value of said plurality of defined power values [the computed power sample at the output of 333 with the

program threshold value in register 335 at 341, the program threshold values are the defined power values; to determined the saturation at 342, for controlling the digitally multiplied gain, Fig. 3, col. 10, lines 29-42 & col. 8, lines 30-37]; the agc 215 is a processor controlled FPGA device, as the code controlled process [col. 7, lines 40-45] & with software programmability, using the code [col. 12, lines 30-32], using the same reasoning in claim 9 above to combine Brobston to Kang.

For claims 11, 37, Kang teaches the computing the accurate rssi 892, but fails to teach the storing said defined power values in a lookup table. Brobston teaches the programmable threshold values are stored in the register 335 as the lookup table [col. 8, lines 27-27]; the agc 215 is a processor controlled FPGA device, as the code control process [col. 7, lines 40-45] & with software programmability, using the code [col. 12, lines 30-32], using the same reasoning in claim 9 above to combine Brobston to Kang.

5. Claims 12, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Oshima et al. (US 2004/0229,586 A1).

For claims 12, 38, Kang fails to teach the further features, the applying a final gain to said received signal.

Oschima teaches the applying a final gain to said received signal [the applying of the final gain code FGC & generating the gain control information based on the difference, 0061-0062, Fig. 19], for accurately control the rest of the gain value based on the preceding gain stage. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang with Oshima's final gain code, in order to accurately control the rest of the gain value based on the preceding gain stage.

6. Claims 13, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Khorramabadi (US 5,864,310).

For claims 13, 39, Kang fails to teach the features for this claim.

Khorramabasi teaches the digital to analog conversion D/A 304 & 304' for converting the samples in register 302, 302' from A/D 218, 218' into plural of time domain signal to remove DC offset at 306, 306' [Fig. 3, col. 4, lines 36-50 & col. 2, lines 30-52], in order to remove the DC offset. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang with Khorramabadi's converting A/D output signal via D/A, in order to remove the DC offset.

7. Claims 14, 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Oschima (US 2003/0218,501 A1).

For claim 14, Kang teaches the steps in Fig. 9, Fig. 11, comprising

generating a plurality of upstream analog signals for a received signal [the down converted signal are output at each VGA of the plural variable gain amplifiers VGA 830, 846, 862 in Fig. 8; col. 8, lines 35-62; as the plural upstream analog signals];

acquiring upstream analog information related to at least a portion of said generated plurality of upstream analog signals [the power detectors 840, 856, 868 detecting, acquiring, the power level at the output of each VGA 830-862, step S910 in Fig. 9, col. 9, lines 30-37; as the acquiring upstream analog information related to a portion of generated upstream analog signals]; and

adjusting a gain for said received signal using at least a portion of said acquired upstream analog information [the reducing the gain of the selected stage, col. 9, lines 34-67 & increasing the gain col. 11, lines 24-37]..

Kang teaches the processor executed code section for the steps in Fig. 9, Fig. 11, but fails to mention the computer program stored in a machine readable storage, for processing signals with the executable code section.

Oschima et al. [Oschima] teaches a machine-readable storage having stored thereon, a computer program having at least one code section for processing received signals in a communication system, the at least one code section being executable by a machine for causing the machine to perform steps [the computer or microprocessor executes instructions stored program software for implementing the gain control method, in paragraph 0068-0070 & gain method in abstract], in order to accurately control the amplifier gain by executing software instructions. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang with Oschima's software instructions, in order to accurately control the amplifier gain by executing software instructions.

For claim 16, Oschima teaches the machine-readable storage having stored computer program in claim 14 above. Kang teaches the wherein said generated plurality of upstream analog signals are narrowband analog signal [the BB filter 836, 852 filtered signal provides the narrow band signal, for the generated plural amplified signals], using the same reasoning in claim 14 above to combine Oschima to Kang.

For claim 17, Oschima teaches the machine-readable storage having stored computer program in claim 14 above. Kang teaches the further comprising code for acquiring at least one sample from at least a portion said generated plurality of upstream analog signals [the measuring power in step s910 & the power detecting power level at PD 820-868 of amplified signal at each VGA output, col. 9, lines 5-22; the received by gain controller 894 & AGC 884

via 876, as the processor], using the same reasoning in claim 14 above to combine Oschima to Kang.

For claim 18, Oschima teaches the machine-readable storage having stored computer program & code in claim 14 above. Kang teaches the computing a power based on said acquired at least one sample [the computing RSSI 892 based on the status gain_rpt 898 from gain controller 899 to gain calibration 899, as processor; the rssi is in dBm, power unit], using the same reasoning in claim 14 above to combine Oschima to Kang.

For claim 19, Oschima teaches the machine-readable storage having stored computer program & code in claim 14 above. Kang teaches the determining when at least one of said generated plurality of upstream analog signals is clipped [the above upper limit of signal level 1020, clipped, the gain controller, as processor, decreases the gain, col. 10, lines 48-58, Fig. 10B], using the same reasoning in claim 14 above to combine Oschima to Kang.

For claim 20. Oschima teaches the machine-readable storage having stored computer program & code in claim 14 above. Kang teaches the generating an intermediate gain based on said computed power of said acquired at least one sample [the intermediate gain change in steps s940 or s950, then process looping upwards to S910, before final gain, Fig. 9], using the same reasoning in claim 14 above to combine Oschima to Kang.

For claim 21, Oschima teaches the machine-readable storage having stored computer program & code in claim 14 above. Kang teaches the applying said generated intermediate gain to said at least one of said generated plurality of upstream analog signals [the reducing the gain stage by predetermined gain step size at s940, s950, Fig. 9, as the applying said intermediate gain], using the same reasoning in claim 14 above to combine Oschima to Kang.

8. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Oschima, as applied to claim 14, and further in view of Khorramabadi-'310.

For claim 26, Kang fails to teach the features for this claim.

Khorramabasi teaches the digital to analog conversion D/A 304 & 304' for converting the samples in register 302, 302' from A/D 218, 218' into plural of time domain signal to remove DC offset at 306, 306' [Fig. 3, col. 4, lines 36-50 & col. 2, lines 30-52], in order to remove the DC offset. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang, Oschima with Khorramabadi's converting A/D output signal via D/A, in order to remove the DC offset.

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Oschima, as applied to claim 14 above, and further in view of Loper (US 5,095,536).

For claim 15, Oschima teaches the machine-readable storage having stored computer program in claim 14 above. It is well known that the low pass filter can be implemented in by software coding, such as the teaching from Loper, the FIR filter in the digital signal processing [co. 12, liens 43-58]. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang, Oschima with Loper's FIR low pass filtering, such that the low pass filter could be convenient relocated for the purpose of processing a signal.

10. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Oshima-'501A1, as applied to claim 18 above, and further in view of Brobston-'409B2.

For claims 22, 23, Kang & Oshima fail to teach the code for comparing said computed power to a plurality of defined power values; the code for selecting gain based on a comparable power value of said plurality of defined power values.

Brobston teaches these features [the computed power sample from output of 333 is compared with the program threshold value in register 335 at 341, the programmable threshold values are the defined power values; to determined the saturation at 342, for controlling, selecting, the digitally multiplied gain, Fig. 3, col. 10, lines 29-42 & col. 8, lines 30-37; the agc for dynamic range in abstract, title], the agc 215 is the processor controlled FPGA device, as the code controlled process [col. 7, lines 40-45] & with software programmability, using the code [col. 12, lines 30-32]. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang, Oshima with Brobston's comparing the calculated power samples to the threshold value, in order to determine & reduce signal saturation.

For claim 24, Kang & Oshima fails to teach the code for storing said defined power value in a lookup table.

Brobston teaches these features [the programmable threshold values are stored in the register 335 as the lookup table in col. 8, lines 27-27]; the agc 215 is a processor controlled FPGA device, as the code controlled process [col. 7, lines 40-45] & with software programmability, using the code [col. 12, lines 30-32], using the same reasoning in claim 9 above to combine Brobston to Kang & Oshima.

11. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Oshima-501A1, as applied to claim 14 above, and further in view of Oshima-'586A1.

For claim 25, Kang & Oshima-'501A1 fails to teach the features for this claim.

Oshima-586A1 teaches the code for applying a final gain to said received signal [the applying of the final gain code FGC & generating the gain control information based on the difference, 0061-0062, Fig. 19], for accurately control the rest of the gain value based on the preceding gain stage. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang, Oshima-501A1 with Oshima's final gain code, in order to accurately control the rest of the gain value based on the preceding gain stage.

12. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Katsura et al. (US 6,373,907 B1) and Sullivan (US 5,451,955).

For claim 40, Kang teaches a system for processing received signals in a communication system [the signals received by antenna 802 in wireless system 800 in Fig. 8 & abstract, the dynamic range in col. 9, lines 11-22], the system comprising

a mixer [816]; a low pass filter [836] coupled to said mixer [816]; and

a plurality of gain controllers [VGA 846-862] serially coupled to an output of said low pass filter [836]; and

Kang teaches the ADC 876 coupled to low pass filter 852, but fails to teach the first of said plurality of analog-to-digital converters ADC is coupled to said output of said low pass filter.

Katsura et al. [Katsura] teaches the wherein an input of a first of said plurality of ADC is coupled to said output of said low pass filter [the first ADC 12 in Fig. 2, coupled to the low pass filter 7, for sampling the signal level at the output of first amplifier 15] before ADC 9.

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang with Katsura's ADC 12, in order to improve the gain controlling by sampling the signal level of the first amplifier output.

Kang & Katsura fail to teach a plurality of analog to digital converters ADC; an input of each remaining portion of said ADC converters is individually coupled to a corresponding output of each serially coupled gain controllers.

Sullivan teaches a plurality of ADC; an input of each of a remaining portion of said plurality of analog-to-digital converters is individually coupled to a corresponding output of each of said serially coupled plurality of gain controllers [plurality of analog to digital converters ADC 28 in Fig. 1 & the remaining ADC 28 are coupled to the output of corresponding amplifiers 14, 16 in Fig. 1], for measuring the subrange power level of the amplifier chain [col. 2, line 65 to col. 4, line 6]. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to upgrade Kang & Katsura with Sullivan's plural of remaining ADC 28 coupled to respective amplifier output to measure each power level, in order to provide subrange power level information from the output of each amplifier.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

A. US 2002/0047,744 A1, Ichihara teaches the serially coupled variable gain amplifiers 102-104, the gaon converting circuit 113, the gain distribution circuit for controlling the gain having limiting value [Fig. 1-5, abstract].

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Chow whose telephone number is (571) 272-7889. The examiner can normally be reached on 8:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Chow C.C.

July 10, 2006.

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